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The Research and Implementation of Sobel Calculatory based on FPGA

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Abstract

The edge of the image carries a lot of important image information. When extracting the edge of the image, it can effectively reduce the amount of data while retaining most of the graphic information. And edge recognition is also the basic technology of image processing and machine vision, especially in the field of image feature extraction. The Sobel operator is an important processing method in the field of image processing, which is mainly used to obtain a degree of digital image. This article uses the dual-core ARM Cortex-A9 processor embedded in the ZYNQ platform to perfectly combine the software programmability with the hardware programmability of the FPGA, uses HLS to achieve Sobel detection, and introduces a new VDMA operation method. The image is displayed in the memory mode, and the system advantages of low power consumption and low cost realize the unparalleled system performance, flexibility, and scalability of a single chip, and accelerate the time to market of graphics processing products.

Keywords

Sobel operator; Field programmable gate array; HLS.

1. INTRODUCTION

With the continuous development of science and technology and the advent of the digital age, the information contained in images has become more abundant. For example, X-ray films and MRI films are often used in medicine, satellite cloud images used in weather monitoring, calligraphy and painting works in the process of artistic creation, and faxes in economic activities. The importance of image processing technology has become increasingly prominent and has gradually attracted people's attention. The edge of the image is the boundary between the image target and the background. It can not only describe the geometric properties of the target's contour, area, perimeter, etc., but also determine the spatial position relationship of the target. Image segmentation, face recognition, and target tracking are all based on image edge detection technology. Edge detection technology, as a basic technology in the field of image analysis, is generally the first step in image analysis. The purpose of edge detection is to detect the location of changes in image features to reflect important changes in the image. Changes in image attributes usually reflect important events or changes in attributes. Common edge detection algorithms are usually divided into two categories: first-order derivative edge detection algorithms and second-order derivative edge detection algorithms, respectively: (1) First-order derivative: Roberts crossover operator, Prewitt operator, Sobel operator (2) Second derivative: LOG operator, Canny operator, Laplacian operator. Among them, Sobel operator is one of the important operators in image edge detection.

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2. THE PRINCIPLE AND REALIZATION OF SOBEL OPERATOR

The Sobel operator is mainly used for edge detection. Technically, it is a discrete difference operator that is used to calculate the approximate value of the gray level of the image brightness function. Using this operator at any point of the image will generate the corresponding gray vector or its normal vector.

The convolution factor of the Sobel operator is:

Table 1. Gx Value

-1	0	+1
-2	0	+2
-1	0	+1

Table 2. Gy Value

+1	+2	+1
0	0	0
-1	-2	-1

The operator contains two sets of 3*3 matrices, which are horizontal and vertical. Convolve them with the image plane to obtain the approximate values of the horizontal and vertical brightness differences.

The horizontal and vertical gray values of each pixel of the image are combined by the following formula to calculate the gray scale of the point:

$$G=\sqrt(G_x^2+G_y^2)$$

If the gradient G is greater than a certain threshold, then (x, y) is considered an edge point.

Then you can use the following formula to calculate the gradient direction:

$$\theta = \tan^{-1}(Gx/Gy)$$

The Sobel operator detects the edge based on the gray-scale weighted difference between the upper and lower, left and right adjacent points of the pixel, and reaches the extreme value at the edge. It has a smoothing effect on noise, provides more accurate edge direction information, and the edge positioning accuracy is not high enough. When the accuracy requirements are not very high, it is a more commonly used edge detection algorithm.

3. HLS IMPLEMENTATION AND VERIFICATION OF SOBEL OPERATOR

3.1. Software and Hardware Collaborative Development Process

OpenCV can be applied in four different ways in the video processing system. In the first method, the design and implementation of the algorithm completely depend on the function call of OpenCV, and the file access function is used to input, output and process the picture; in the second method, the algorithm can be used in an embedded system (such as Zynq Base TRD).)), use the function call of a specific platform to access the input and output images, but the realization of video processing depends on the call of the OpenCV function function of the

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processor (such as CortexT-A9) in the embedded system; in the third way, processing The OpenCV function of the algorithm is replaced by the Xilinx Vivado HLS video library function, and the OpenCV function is used to access the input and output images and provide a design prototype for the realization of the video processing algorithm. The video library functions provided by Vivado HLS can be synthesized. After synthesizing these functions, the processing program module can be integrated into programmable logic such as Zynq. In this way, these program logic blocks can process the video stream produced by the processor, the data read from the file, and the real-time video stream input from the outside.

Vivado HLS contains a large number of video library functions to facilitate the construction of various video processing programs. Through synthesizable C++ code, these video library functions are realized. In terms of video processing functions and data structure, these integrated codes basically correspond to OpenCV. Many video concepts are very similar to abstraction and OpenCV, and many image processing module functions are consistent with OpenCV library functions.

3.2. Build A Hardware System

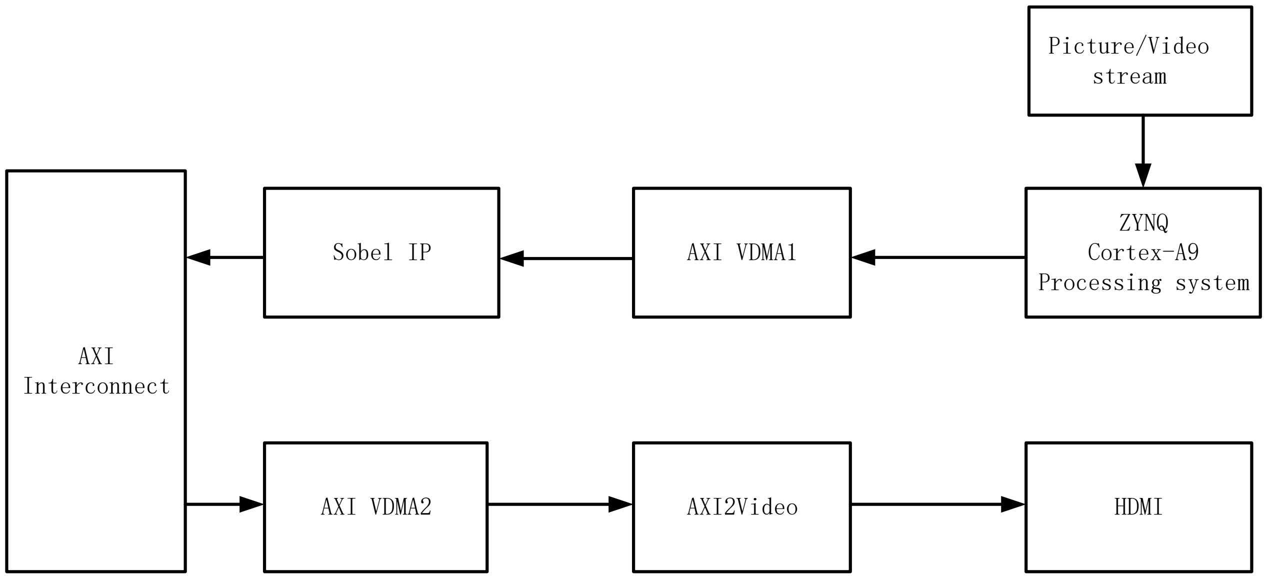

Figure 1. System hardware design block diagram

3.3. HLS Software Implementation Scheme

After the vivado is integrated, the system hardware project will generate a BSP board support package while generating the PL hardware bit stream. The physical address information of each functional IP core connected to the PS through the AXI4-Lite bus inside the PL is included in This BSP board support package. The system driver software realizes functions such as initial configuration of each IP core and communication control based on the address information in the BSP package.

The system software is designed based on the SDK development platform that comes with Vivado and is programmed in C language. First of all, after the system is powered on, the PS starts first, initializes the hardware platform, initializes the IO input and output interfaces, and initializes each IP core. After the configuration is completed, the IP core of the PL part starts to enter the normal working mode, and the PS part enters the working mode. Allocate the read and write buffer of VDMA, take the modulus of the test picture through Imager2LCD software, convert the pixels into a 32-bit C language array, and use it as the input of VDMA. In this project, two VDMA modules are used, of which VDMA has only one write channel, which is responsible for the display cache function, and VDMA1 has two channels, which are responsible for sending our modulo array to the memory and the data cache after sobel processing. The role of. So three

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buffers are allocated here to store the data of the three channels respectively. After the processing is completed, the VDMA0 module converts the processed data into video data through the AXI4-Stream interface, and displays it on the screen through the HDMI interface.

4. BOARD-LEVEL VERIFICATION AND DEBUGGING

After compiling with the vivado SDK software, download the program to the black gold development board, and get the following results:

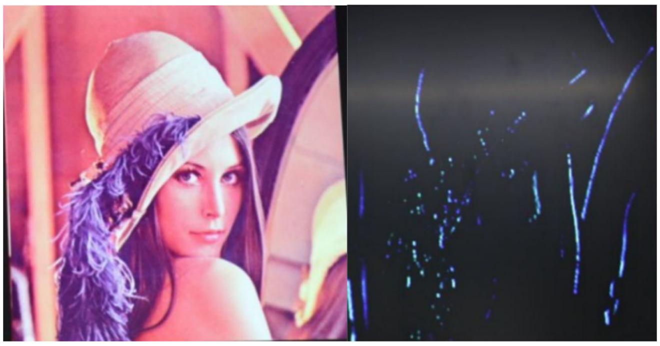

Figure 2. Original Picture and Picture processed by edge detection

5. CONCLUSION

Aiming at the disadvantages of long delay and limited data bandwidth in traditional OpenCV image processing, hardware acceleration can make up for the shortcomings. Using VivadoHLS to further realize the hardware circuit design on the basis of software application, greatly shortening the development cycle of the system. This article not only proposes a hardware acceleration scheme for edge detection, but also proposes a scheme for system design through the combination of software and hardware in applications with large data processing volume and fast processing speed. The design is verified based on the zynq series FPGA chip xc7z020clg484 of Xilinx Company, and the hardware test is carried out on the black gold development board. The simulation results verify the simplicity and effectiveness of the model.

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